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EUV 3.0

High NA a prime Digital Enabler for the next decade with deep competitive moat

In the context of the **$600bn global semiconductor market, which is estimated to reach over $1trn by 2030**, we see **High NA, the next generation of Extreme Ultraviolet Lithography (EUV)** with ASPs of €300-400mn (c2x that of EUV), as a key **European Digital Enabler** facilitating use cases such as **AI, HPC and autonomous driving.** This technology delivers higher resolution by using improved optics, which we see as **crucial in supporting continued lithography growth momentum beyond 2025** and into the next decade. Our work (including EUV expert calls and lithography HQ visits) suggests that
1) a significant market for High NA will emerge across 2025-30 (as the increasing proliferation of **advanced semis applications such as AI** drives customer willingness to pay for more complex and powerful lithography tools); **2)** the **future High NA roadmap is meaningfully de-risked** and should not face the same commercialisation challenges as EUV initially did (but will still be extremely difficult for a competitor to replicate for the next 10-20 years at least); and **3)** transformative architectural transitions (such as the shift to **Gate-All-Around or chiplets) will not derail High NA insertion** post 2025, but instead will complement advanced lithography going forward by facilitating further chip shrink and complexity.

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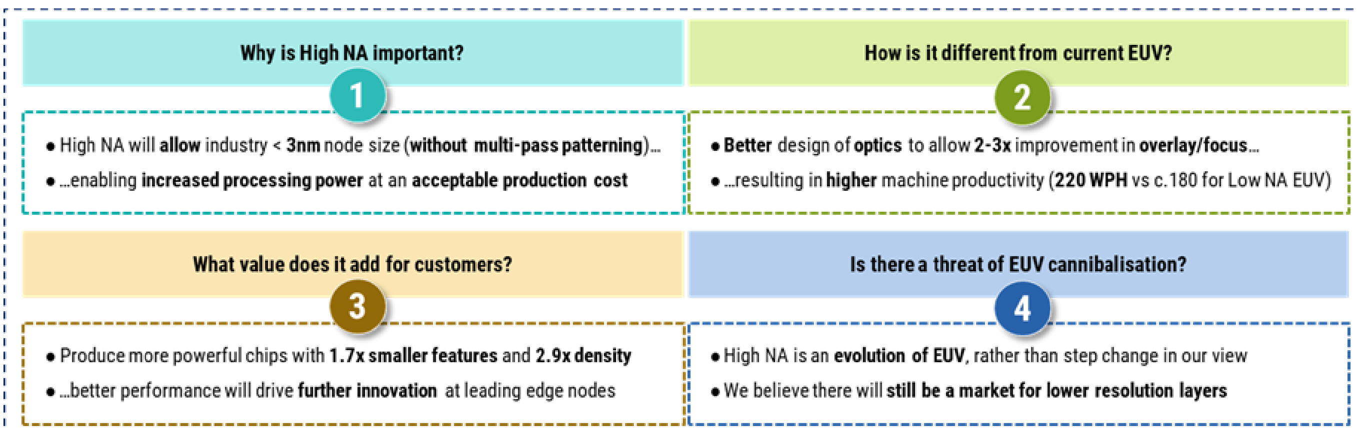
In the context of the **$600bn global semiconductor market, which is estimated to reach over $1trn by 2030**), we see **High NA, the next generation of Extreme Ultraviolet Lithography (EUV)** with ASPs of €300-400mn (c2x that of EUV), as a **key European Digital Enabler** facilitating use cases such as **AI, HPC** and **autonomous driving**. This technology delivers higher resolution by using improved optics, which we see as **crucial in supporting continued lithography growth momentum beyond 2025** and into the next decade.

- At the time of our previous deep-dive report in September 2021, key investor debates centered on the state of EUV adoption towards the middle of the decade, alongside the likely implications for trailing-edge Deep Ultraviolet (DUV) lithography machines. Following adoption of EUV that has been faster than our expectations at both Logic and Memory customers, we believe the **focus of the debate will shift towards the next-generation of EUV lithography tools (i.e. High NA).**
- Our work (including EUV expert calls and lithography HQ visits) suggests that **1)** a **significant market for High NA will emerge across 2025-30** (as the increasing proliferation of **advanced semis applications such as AI** drives customer willingness to pay for more complex and powerful lithography tools); **2)** the future **High NA roadmap is meaningfully de-risked** and should not face the same commercialisation challenges as EUV initially did (but will benefit from the same extremely high barriers to entry); and **3)** transformative architectural transitions (such as the shift to **Gate-All-Around or chiplets) will not derail High NA insertion** post 2025, but instead will complement advanced lithography going forward by facilitating further chip shrink and complexity, in turn catalysing a higher absolute level of spending on advanced chip nodes (contrasting some investor concerns in this area).

High NA, the next generation of EUV tools that delivers higher resolution by using improved optics

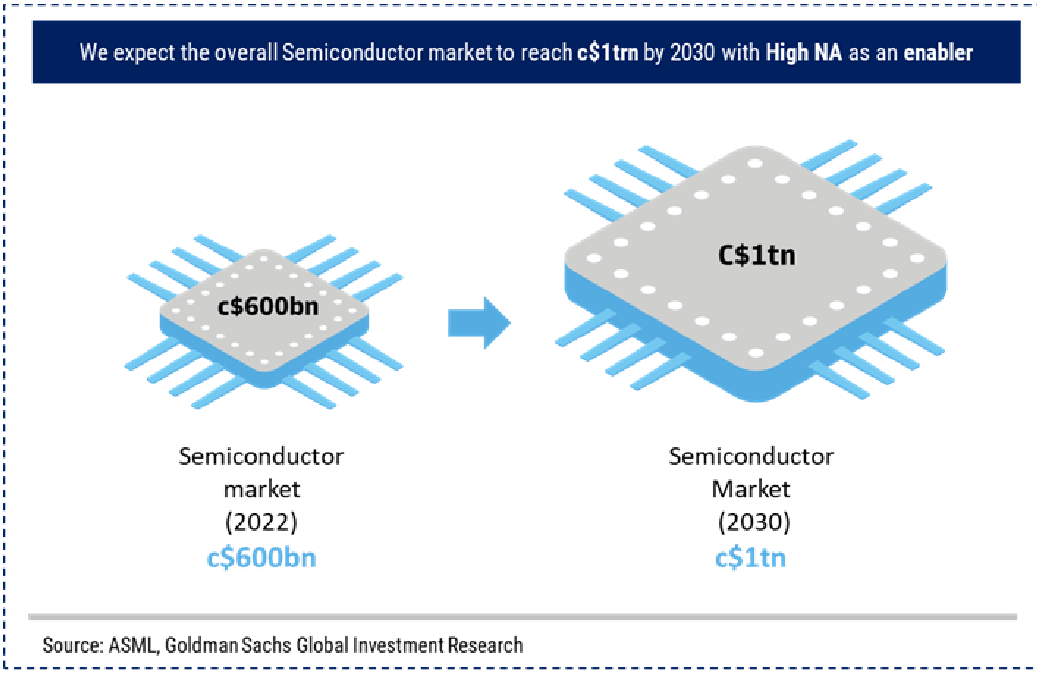
We believe that **High NA, which is the next generation of Extreme Ultraviolet Lithography (EUV) that delivers higher resolution by using improved optics,** will be crucial in supporting continued lithography growth momentum beyond 2025 and into the next decade, thereby warranting **characterisation as a key Digital Enabler** in our view. Importantly, these tools will **provide a path on EUV to industry 3nm and below in our view, obviating the need for expensive multiple pass patterning on low NA EUV** (as Low NA EUV did for Immersion Lithography). Therefore, we believe High NA will be critical in facilitating the production of advanced semis needed for AI, 5G and high-performance computing at an acceptable cost, thereby helping to **drive the global semis market towards a c$1trn level by 2030.**

Exhibit 1: High NA will provide a path on EUV to industry 3nm and below in our view, obviating the need for expensive multiple pass patterning on low NA EUV



Source: Company data, Goldman Sachs Global Investment Research

Exhibit 2: We believe High NA will be crucial in facilitating the production of advanced semis needed for AI, 5G and high-performance computing at an acceptable cost, thereby helping to drive the global semis market towards a c$1trn level by 2030



Source: ASML, Goldman Sachs Global Investment Research

Future High NA roadmap is meaningfully de-risked and should not face the same commercialisation challenges as EUV, thereby supporting a robust level of long-term adoption

We believe that **maturity of the High NA product at launch will be higher than initially was the case for EUV historically,** helping to reduce the risk of roadmap delays on High NA, contrasting some investor concern that the product could see similar industrialisation challenges that delayed the prior commercial launch of low NA EUV by several years. Given that **High NA is an extension of the EUV process**, we see fewer risks involving in commercialising High NA in a timely manner, supporting a faster rate of near-term customer adoption.

- **High NA will involve a new lens system** (produced by Carl Zeiss, similar to EUV), which will have a **higher numerical aperture in order to achieve finer printing** and more accurate optics. Moreover, the new design will minimise the number of mirrors required to reflect EUV light (to maximise productivity), and utilise an anamorphic lens for the first time (for better control over magnification and accuracy).
- In order to offset the smaller image field size offered by the new finer lens, **ASML will incorporate faster scanning stages** (on which the wafer and reticle sit), which will facilitate a timely scanning process. While managing the faster acceleration will require meaningful engineering competence, we note that **these stages will already be introduced within the 3800E low NA EUV system,** which we believe helps to de-risk the ramp of this component.
- While we characterise the upgrades to the lens system as quite transformative, we note that ASML has already spent several years developing and industrialising low NA EUV, with **High NA using several technologies that will already be industrialised in low NA EUV** e.g. same source, wavelength of light, drive laser etc, suggesting that the **key fundamental challenge will be the higher numerical aperture** in our view. We believe this **commonality (to low NA EUV) will help to lower the manufacturing risk associated with High NA**, given that it is an extension of a process on which ASML already possesses deep knowledge and practical expertise, as well as somewhat preparing the supply chain for the ramp of High NA modules. As such, we **characterise the technological steps for High NA as evolutionary rather than revolutionary**, reducing the risk of roadmap delays and supporting a faster rate of near-term customer adoption in our view.

Exhibit 3: We characterise the technological steps for High NA as evolutionary rather than revolutionary

	Large change?	Evolution?	Broadly similar?	Most development items involve an evolution of EUV, rather than a step change
1 Laser			✓	• High NA uses the **same light source as standard EUV light**
2 Optics	✓			• Carl Zeiss to **develop larger mirrors/lenses for High NA** to boost numerical aperture, albeit **Zeiss/ASML** already have a strong **working relationship**
3 EUV Light			✓	• **Same wavelength of light** (13.5nm) used to print on wafer as standard EUV; **better** granularity enabled by **higher resolution** optics
4 Moving Platform		✓		• **Higher performance moving platform** (scanning stage) required, this **wafer stage** will be introduced in **3800E tools**, which we believe helps to de-risk
5 General Productivity		✓		• Some **new challenges** in interfacing with **new cables/signals**, better environmental conditioning • Engineering of key processes (e.g.**in-situ cleaning), already innovated for EUV**

Source: Company data, Goldman Sachs Global Investment Research

Separately, following our latest expert call on EUV, we believe that **successful introduction** of **High NA** is further safeguarded by the **high barriers** to entry which exist in the Lithography market (especially for EUV tools).

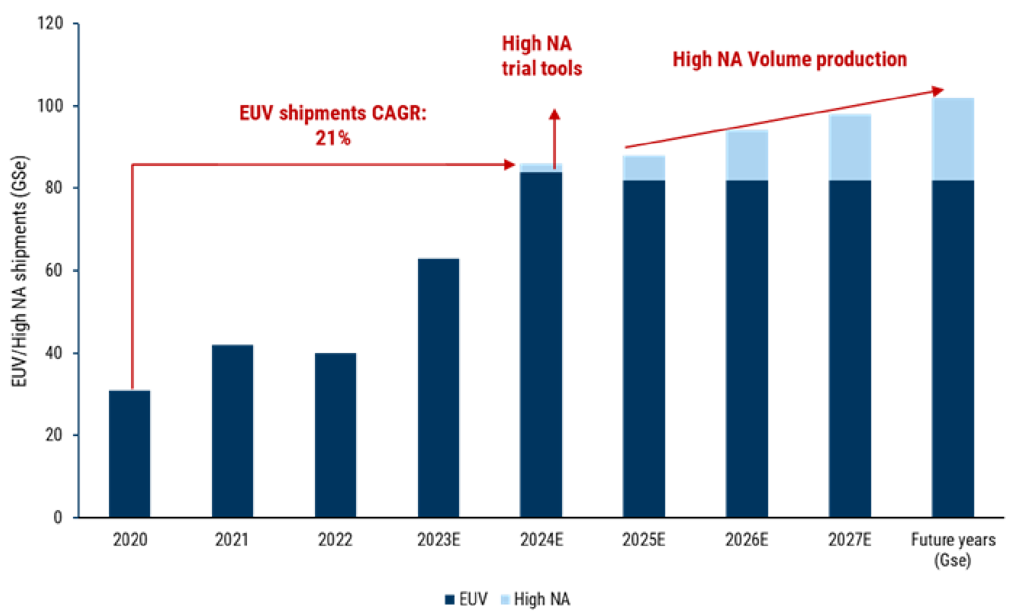
Given that it has **not yet become necessary to perform costly and inefficient multiple pass patterning on EUV** (as was the case on DUV by the time of EUV's introduction), which creates extra cost given the additional steps in the manufacturing process, **we do not expect a high degree of cannibalisation of Low NA EUV by High NA**, resulting in relatively sustained demand for regular EUV machines even as High NA ramps.

- As **advanced use cases continue to proliferate (e.g. AI),** we believe smaller and more powerful chips will be required to support leading edge technology. However, at smaller process nodes, semiconductor circuitry also becomes more complex,

Moreover, we believe that **High NA will be critical in supporting the proliferation of leading-edge semis applications (such as advanced AI**, for which both cutting-edge Logic *and* DRAM is required), which we see as an incremental driver to ASML's addressable lithography market, supporting a ***co-existence*** **between EUV and High NA** in our view.

- In particular, we anticipate that **AI will be a strong High NA demand driver for both Logic *and* Memory customers,** given AI's need for **extremely fast processing (ie. Logic), greater and faster data storage (ie. DRAM)**.
- Furthermore, we note that the **proliferation of leading-edge use cases is also likely to catalyse incremental demand for non-High NA lithography tools** as well given that 1) a range of **MCs, power semis, analog semis and image sensors are required to enable the functioning of advanced applications**, which often rely on Dry/Immersion lithography and 2) an advanced chip can consist of c100 layers, of which **only the most complex layers will use EUV/High NA,** driving incremental demand for new Immersion/Dry applications on the remaining layers as well, which could support higher long-term demand for other mature lithography technologies in our view.

Exhibit 4: We believe that certain new semis applications (e.g. for advanced AI) will emerge that require transistor features that are so small and complex, such that High NA could be the only cost effective lithography solution for such designs.



Source: Company data, Goldman Sachs Global Investment Research

Latest customer commentary and regulatory support suggests robust dynamics for leading-edge chip investments in coming years, from which we expect High NA to benefit

We believe dynamics surrounding the **geopolitics and protection of technological sovereignty** could accelerate the efforts of customers to diversify manufacturing regionally, which, in our view, could cause **higher capex/spending inefficiency** and hence **benefit the lithography market by creating additional demand for more tools** (alongside demand for other semicap equipment). Recently ASML highlighted that it expects technological sovereignty to increase inefficiencies in manufacturing and **expand the demand of wafers by c.10%,** which will in turn need to be met with a higher level of global manufacturing capacity.

- We see initiatives such as the **US and EU Chips Act** as examples of regions aiming to re-shore certain critical manufacturing processes in order to **protect technological sovereignty** and, to some degree, helping to ensure domestic supply. These initiatives aim to **accelerate domestic production** of critical semis by providing tax subsidies and federal investments, and maintain tech sovereignty in the country by restricting exports to certain regions. .
- **South Korea** and **Taiwan** have also taken steps to support domestic semiconductor manufacturing capabilities by aiming to **provide tax incentives** and **additional support to set up manufacturing facilities**. We detail such initiatives in the below exhibit.
- In our view, **efforts to protect technological sovereignty have the effect of diversifying manufacturing globally**, which we believe could cause higher capex/spending inefficiency (as it could be less efficient for production to be split across clean rooms in multiple geographies), hence benefiting the lithography market (such as High NA, alongside other semicap spending areas) by creating additional demand for more tools. We see High NA a key beneficiary given its key application is leading-edge chip processes, which are often considered among the most strategic chip markets by global governments.

Exhibit 5: Governments across the globe are incentivising a more localised semis supply chain, which we expect to increase the inefficiencies in production and positively impact the demand for ASML's Lithography tools (including High NA)

Government initiatives across the globe are encouraging a more localised semis supply chain	

US Chips Act (United States)	• The **CHIPS and Science Act** provides **$52.7bn** for **American** semiconductor **R&D**, **manufacturing**, and **workforce development**
	  • It includes **$39bn** in **manufacturing incentives**, including **$2bn** for **legacy chips for automobiles** and defense systems
	  • Additionally, the act provides **$13.2bn in R&D and workforce development**
	• It also includes a **25% investment tax credit** for capex for manufacturing of semiconductors and related equipment
	• Beneficiary: E.g. **Micron** plans to invest **c$40bn** in US by the end of decade driven by incentives from the Chips Act (GSe)

EU Chips Act (European Union)	• The **EU Chips ACT** will mobilise **>€43bn** of **public and private investments** to strengthen **Europe's technological leadership**
	  • It aims to **strengthen Europe's** research and technology **leadership** towards **smaller and faster chips**
	  • Establish a framework to **increase production capacity to 20%** of the global market by **2030**
	• The act will focus on semiconductor international partnerships with like-minded countries
	• Beneficiary: E.g. **Intel** is expected to receive government **incentives** of **c€10bn** as part of EU Chips Act

K-Chips Act (South Korea)	• The **K-Chips Act** will increase **corporate tax break** for domestic facility investment in strategic industries like semiconductors • **Tax break** for **large-sized corporations** will increase **to 15% from 8**%; **SMEs** it will increase **to 25% from 16%** • Additional **10% tax break** for amount of **investment** made in **current year** that exceeds the **average amount** during past **3-years** • It will incentivize domestic semiconductor investment for Korean companies and help strengthen the domestic supply chain • Beneficiary: E.g. **Samsung** is expected to maintain its **capex intensity** for being eligible for **10% additional tax breaks** (GSe)

Invest Taiwan Initiative (Taiwan)	• The **Invest Taiwan Initiative** is focused on maintaining **Taiwan's leading position** in global semis supply chain
	  • The Act states that for profit-seeking enterprise **income tax rate is 20%**
	  • Further, up to**15%** of the **R&D expenditure** may be **deducted** from profit-seeking enterprise **income tax** for current year
	  • Additionally, the Act will support companies in **securing land, water and electricity** for setting up fabs
	• Beneficiary: E.g. **TSMC** is expected to continue its production expansion in Taiwan

Disclosure Appendix

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